IN THE CLAIMS

Please amend the claims as follows:

1. (previously presented) A digital signal transmission system comprising:

a first driver circuit receiving a first data input signal and generating a first driver output signal in response to a clock signal, said first driver output coupled to a first input of a first transmission line;

a receiver circuit having a first receiver input coupled to a first output of said first transmission line and a second receiver input coupled to a reference voltage; and

a first terminating network receiving programming signals and generating a first terminating voltage with a first source impedance at a first node, said first node coupled to said first output of said first transmission line, wherein said first terminating voltage is modified in response to said programming signals while maintaining a pre-determined magnitude of said first source impedance.

2. (previously presented) A digital signal transmission system comprising:

a first driver circuit receiving a first data input signal and generating a first driver output signal in response to a clock signal, said first driver output coupled to a first input of a first transmission line;

a receiver circuit having a first receiver input coupled to a first output of said first transmission line and a second receiver input coupled to a reference voltage;

a first terminating network receiving programming signals and generating a first terminating voltage with a first source impedance at a first node, said first node coupled to said first output of said first transmission line, wherein said first terminating voltage is modified in response to said programming signals while maintaining a pre-determined magnitude of said first source impedance;

a second driver circuit receiving said clock signal and generating a first clock output signal coupled to a second input of a second transmission line;

a second terminating network generating a second terminating voltage with said first source impedance at a second node, said second node coupled to a second output of said second transmission line;

a third driver circuit receiving said clock signal and generating a second clock output signal coupled to a third input of a third transmission line, said second clock output signal a complement of said first clock output signal;

a third terminating network generating a third terminating voltage with said first source impedance at a third node, said third node coupled to a third output of said third transmission line; and

a filter network receiving said second and third outputs and generating said reference voltage.

3. (original) The digital signal transmission system of claim 2, wherein said filter network comprises:

a first resistor coupled to said second output and to a reference node;

a second resistor coupled to said third output and said reference node; and

a capacitor coupled to said reference node and at least one potential of said second power supply voltage, said reference node generating said reference voltage.

4. (previously presented) The digital signal transmission system of claim 2, wherein said first terminating network comprises:

a number N resistor voltage divider circuits each having an output node, a positive voltage node, and a negative voltage node;

a first electronic switch coupled from each one of said positive voltage nodes to a positive potential of a power supply voltage, each of said first electronic switches controlled by one of said programming signals; and

a second electronic switch coupled from each one of said negative voltage nodes to a negative potential of said power supply voltage, each of said second electronic switches controlled by said corresponding one of said programming signals, wherein

each of said first electronic switches couples said first voltage to one of said positive voltage nodes in response to a first state of said one of said programming signals and each of said second electronic switches couples said second voltage to one of said negative voltage nodes in response to a second state of said corresponding one of said programming signals, and wherein said output nodes of each of said plurality of voltage divider networks are coupled forming said first node, said first node generating said first terminating voltage with said corresponding first source impedance.

5. (previously presented) The digital signal transmission system of claim 2, wherein said first terminating voltage is modified in a number M integer increments.

6. (previously presented) The digital signal transmission system of claim 5, wherein said number N corresponds to a minimum number of said N resistor voltage divider networks necessary to generate said M integer increments of said first terminating voltage.

7. (previously presented) A digital signal transmission system comprising:

a driver circuit in a first integrated circuit (IC) receiving a data signal and generating a data signal output, said data signal output coupled to a first input of a first transmission line;

a termination network in a second IC receiving programming signals and generating a termination voltage having a first source impedance in response to said programming signals at a termination node, wherein said termination node is coupled to an output of said first transmission line;

a differential receiver in said second IC having a second input coupled to said termination node and a third input coupled to a reference voltage; and

a reference network receiving a first clock transmitted from said first IC with a second transmission line, a second clock transmitted from said first IC with a third transmission line, and said programming signals and, generating said reference voltage in response to the first and second clock, wherein said terminating voltage is varied in

response to said programming signals while maintaining a pre-determined magnitude of said first source impedance.

8. (original) A method for optimizing a noise margin in a digital signal transmission system comprising the steps of:

transmitting a data signal on a first transmission line at transitions of a clock signal;

receiving an output of said first transmission line at a first input of a differential input receiver, said first input coupled to a first node of a terminating network receiving programming signals and generating a first terminating voltage with a first source impedance at said first node;

coupling a second input of said differential receiver to a reference voltage;

modifying said terminating voltage in response to said programming signals;

monitoring an output of said differential receiver for a quality of a received data signal; and

setting said first terminating voltage at an optimized level corresponding to said quality of said received data signal.

9. (original) The method of claim 8 further comprising the steps of:

transmitting said clock signal on a second transmission line terminated at a second node of a second termination network generating a second terminating voltage with a second source impedance at said second node;

transmitting a complement of said clock signal on a third transmission line terminated at a third node of a third termination network generating a third termination voltage with a third source impedance at said third node; and

coupling said second and third node to a reference node using a first filter network, said reference node generating said reference voltage.

10. (original) The method of claim 8, wherein said first source impedance remains fixed during said step modifying of said terminating voltage.

11. (previously presented) A data processing system comprising:

a processor central processing unit (CPU) integrated circuit (IC) chip operable to transmit off-chip signals, having circuitry for transmitting a digital signal on a first transmission line corresponding to edges of a clock signal, circuitry for terminating said first transmission line in a programmable terminating voltage having a source impedance, said programmable terminal voltage modified in response to first program signals, and

circuitry for receiving said digital signal at a first receiver input coupled to said programmable terminal voltage and an output of said first transmission line, receiving a reference voltage at a second receiver input coupled, and generating a receiver output;

a random access memory (RAM); and

a bus system coupling said CPU to said RAM, wherein said terminal voltage is modified while controlling the magnitude of said source impedance to optimize said received digital signal.

12. (currently amended) A data processing system comprising:

a processor central processing unit (CPU) integrated circuit (IC) chip operable to transmit off-chip signals, having circuitry for transmitting a digital signal on a first transmission line corresponding to edges of a clock signal, circuitry for terminating said first transmission line in a programmable terminating voltage having a source impedance, said programmable terminal voltage modified in response to first program signals, and

circuitry for receiving said digital signal at a first receiver input coupled to said programmable terminal voltage and an output of said first transmission line, receiving a reference voltage at a second receiver input coupled, and generating a receiver output;

a random access memory (RAM);

a bus system coupling said CPU to said RAM, wherein said terminal voltage is modified while controlling the magnitude of said source impedance to optimize said received digital signal; ~~The data processing system of claim 11 comprising:~~

circuitry for transmitting said clock signal on a second transmission line;

circuitry for transmitting a complement of said clock signal on a third transmission;

circuitry for terminating said clock signal at a second output of said second transmission line;

circuitry for terminating said complement clock signal at a third output of said third transmission line; and

circuitry for coupling said second output and said third output to said reference voltage, wherein said reference voltage is modulated by a selected frequency content of said clock signal and said complement clock signal.

13. (original) A signal transmission system comprising:

circuitry for transmitting a digital signal on a first transmission line corresponding to edges of a clock signal;

circuitry for terminating said first transmission line in a programmable terminal voltage having a source impedance, said programmable terminal voltage modified in response to first program signals; and

circuitry for receiving said digital signal in a first receiver input coupled to said programmable terminal voltage and an output of said first transmission line and generating a receiver output in response to said received digital signal and a reference voltage coupled to a second receiver input, wherein said programmable terminating voltage is modified to optimize said received digital signal.

14. (currently amended) A signal transmission system comprising:

circuitry for transmitting a digital signal on a first transmission line corresponding to edges of a clock signal;

circuitry for terminating said first transmission line in a programmable terminal voltage having a source impedance, said programmable terminal voltage modified in response to first program signals;

circuitry for receiving said digital signal in a first receiver input coupled to said programmable terminal voltage and an output of said first transmission line and generating a receiver output in response to said received digital signal and a reference voltage coupled to a second receiver input, wherein said programmable terminating voltage is modified to optimize said received digital signal; ~~The signal transmission system of Claim 13 comprising:~~

circuitry for transmitting said clock signal on a second transmission line;

circuitry for transmitting a complement of said clock signal on a third transmission;

circuitry for terminating said clock signal at a second output of said second transmission line;

circuitry for terminating said complement clock signal at a third output of said third transmission line; and

circuitry for coupling said second output and said third output to said reference voltage, wherein said reference voltage is modulated by a selected frequency content of said clock signal and said complement clock signal.

15 (previously presented) A digital signal transmission system comprising:

a first driver circuit receiving a first data input signal and generating a first driver output signal in response to a clock signal, said first driver output coupled to a first input of a first transmission line;

a receiver circuit having a first receiver input coupled to a first output of said first transmission line and a second receiver input coupled to a reference voltage; and

a first terminating network receiving programming signals and generating a first terminating voltage with a first source impedance at a first node, said first node coupled to said first output of said first transmission line, said first terminating voltage modified in response to said programming signals while maintaining a pre-determined magnitude of said first source impedance,

wherein said first terminating network has a number N resistor voltage divider circuits each having an output node, a positive voltage node, and a negative voltage node,

a first electronic switch coupled from each one of said positive voltage nodes to a positive potential of a power supply voltage, each of said first electronic switches controlled by one of said programming signals, and a second electronic switch coupled from each one of said negative voltage nodes to a negative potential of said power supply voltage, each of said second electronic switches controlled by said corresponding one of said programming signals, wherein each of said first electronic switches couples said first voltage to one of said positive voltage nodes in response to a first state of said one of said programming signals and each of said second electronic switches couples said second voltage to one of said negative voltage nodes in response to a second state of said corresponding one of said programming signals, and wherein said output nodes of each of said plurality of voltage divider networks are coupled forming said first node, said first node generating said first terminating voltage with said corresponding first source impedance.

16. (previously presented) The digital signal transmission system of claim 14, wherein said first terminating voltage is modified in a number M integer increments.

17. (previously presented) The digital signal transmission system of claim 16, wherein said number N corresponds to a minimum number of said N resistor voltage divider networks necessary to generate said M integer increments of said first terminating voltage.